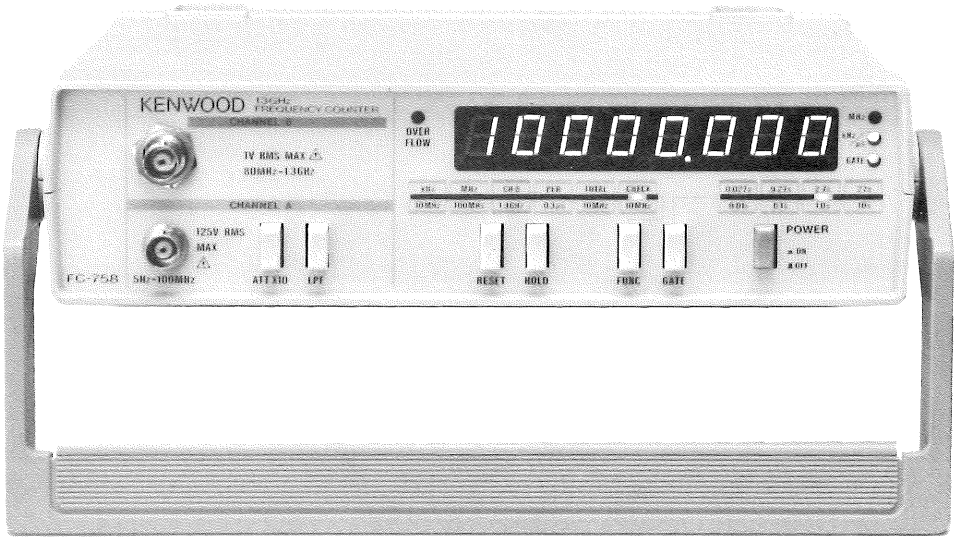
KENWOOD

1.3GHz FREQUENCY COUNTER

FC-758

SERVICE MANUAL

KENWOOD CORPORATION



WARNING

The following instructions are for use by qualified personnel only. To avoid electric shock, do not perform any servicing other than contained in the operating instructions unless you are qualified to do so.

CONTENTS

SPECIFICATION

	FC-758
Frequency Measurement (Channel A)	
Measurement Range	kHz mode: 5 Hz to 10 MHz MHz mode: 5 Hz to 100 MHz
Accuracy	±Reference Time Accuracy ±1 count
Resolution	kHz mode: 0.1 Hz to 100 Hz MHz mode: 1 Hz to 1000 Hz
Counting time (Gate time)	0.01s, 0.1s, 1.0s, 10.0s
Unit	kHz, MHz
Frequency Measurement (Channel B)	
Measurement Range	80 MHz to 1.3 GHz
Accuracy	± Reference Time Accuracy ±1 count
Resolution	Prescale: 10 Hz to 10 kHz
Counting Time (Gate Time)	0.027s, 0.27s, 2.7s, 27s
Unit	MHz
Period Measurement (A)	
Measurement Range	0.285 μs to 200 ms (5 Hz to 3.5 MHz)
Accuracy	±1 count ± Reference Time Accuracy ± Trigger Error*[1]
Resolution	100 ps to 100 ns
Unit	μs
Minimum Pulse Width	142.5 ns
Magnification (Gate Time)	×1, ×10, ×100, ×1000
Totalize Measurement (A)	
Measurement Range	5 Hz to 10 MHz
Maximum Total Count	0 to 99, 999, 999
Control Method	Reset/Hold control from the front panel. Always active except for the case where the Start/Stop input terminal level is 'InActive (active high).
Input Characteristics (Channel A)	
Frequency Band Width	5 Hz to 100 MHz (Coupling: AC coupling)
Sensitivity (sine wave)	kHz mode: 20mVr.m.s. (5 Hz to 10 MHz) MHz mode: 20mVr.m.s. (5 Hz to 30 MHz) 50mVr.m.s. (30 MHz to 100 MHz)
Impedance	1.2 MΩ, 40 pF or less
Maximum Input Voltage	125Vr.m.s. at 400 Hz
Attenuation	×1 (1/1), ×10 (1/10)
Low Pass Filter	100 kHz, −3 dB
Input Characteristics (Channel B)	
Frequency Band Width	80 MHz to 1.3 GHz (Coupling: AC coupling)
Sensitivity (sine wave)	10mVr.m.s. (80 MHz to 600 MHz) 25mVr.m.s. (600 MHz to 1.0 GHz) 50mVr.m.s. (1.0 GHz to 1.3 GHz)
Impedance	50 Ω
Maximum Input Voltage	1.5Vr.m.s.

SPECIFICATION

	FC-758
Reference Oscillator	
Oscillation Frequency	Crystal Oscillation 10.0 MHz (Channel A: 5 Hz to 100 MHz) Crystal Oscillation 3.90625 MHz (Channel B: 80 MHz to 1.3 GHz)
Stabilization (Temperature Factor, Aging Rate)	3×10^{-6}/0 to 40°C (10.0 MHz) 1×10^{-6}/0 to 40°C (3.90625 MHz) 5×10^{-7}/Month (10.0 MHz) 2×10^{-7}/Month (3.90625 MHz)
Display Function	
Display	Eight-digit 7-segment LED Display kHz/μs, MHz, GATE, OVER FLOW
Functions Display	kHz, MHz, CH B, PER, TOTAL, CHECK
Counting Time (Gate time)	CH A: 0.01s, 0.1s, 1.0s, 10s CH B: 0.027s, 0.27s, 2.7s, 27s
Self-check Function	
Display	Display a count value of the internal time base timer (10.0 MHz)
Counting Time (Gate time)	0.01s, 0.1s, 1.0s, 10s
Resolution	0.1 Hz to 100 Hz
General Requirements	
Power supply voltage Power Comsunption	100/120/220/240 V ± 10% (Max. 250 V), 50/60 Hz 20 VA
Within Specifications Temperature and Humidity	23°C ± 5°C, 70%RH
Operating Temperature and Humidity	0°C to 40°C, 80%RH
Dimentions	240(W) × 64(H) × 190(D) mm [Max. 260(W) × 70(H) × 210(D) mm]
Weight	1.8 kg
Accessories	Instruction Manual 1 Power Supply Cable 1 Replacement Fuse 1

*1 Trigger error is typically ±0.3% of reading divided by the number of cycles averaged, for input signals having better than 40 dB S/N ratio and greater than 100 mV amplitude.

SAFETY

SAFETY

Before connecting the instrument to a power source, carefully read the following information, then verify that the proper power cord is used and the proper line fuse is installed for power source. The specified voltage is shown nearly at the AC inlet. If the power cord is not applied for specified voltage, there is always a certain amount of danger from electric shock.

Line voltage

This instrument operates using ac-power input voltages that 100/120/220/240 V at frequencies from 50 Hz to 60 Hz.

Power cord

The ground wire of the 3-wire ac power plug places the chassis and housing of the instrument at earth ground. Do not attempt to defeat the ground wire connection or float the instrument; to do so may pose a great safety hazard.
The appropriate power cord is supplied by an option that is specified when the instrument is ordered.
The optional power cords are shown as follows in Fig. 1.

Line fuse

The fuse holder is located on the rear panel and contains the line fuse. Verify that the proper fuse is installed by replacing the line fuse.

Voltage conversion

This instrument may be operated from a 100 V to 240 V, 50/60 Hz power source. Use the following procedure to change from 100 to 240 volt operation or vice versa.

1. Remove the fuse holder.
2. Replace fuse F 5 with a fuse of appropriate value, 0.25 amp for 100 VAC to 120 VAC operation, 0.125 amp for 220 VAC to 240 VAC operation.
3. Reinsert it for appropriate voltage range.
4. When performing the reinsertion of fuse holder for the voltage conversion, the appropriate power cord should be used. (See Fig. 1.)

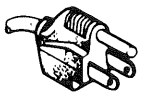
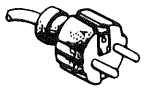
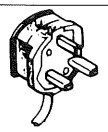
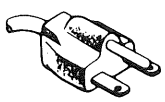
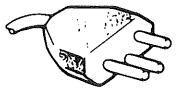
Plug configuration	Power cord and plug type	Factory installed instrument fuse	Line cord plug fuse	Parts No. for power cord and plate
	North American 120 volt/60 Hz Rated 15 amp (12 amp max; NEC)	0.25 A, 250 V Slow blow 6×30 mm	None	Cord: E30-1820-05
	Universal Europe 220 volt/50 Hz Rated 16 amp	0.125 A, 250 V Slow blow 6×30 mm	None	Cord: E30-1819-05
	U.K. 240 volt/50 Hz Rated 13 amp	0.125 A, 250 V Slow blow 6×30 mm	0.8 A Type C	—
	Australian 240 volt/50 Hz Rated 10 amp	0.125 A, 250 V Slow blow 6×30 mm	None	Cord: E30-1821-05
	North American 240 volt/60 Hz Rated 15 amp (12 amp max; NEC)	0.125 A, 250 V Slow blow 6×30 mm	None	—
	Switzerland 240 volt/50 Hz Rated 10 amp	0.125 A, 250 V Slow blow 6×30 mm	None	—

Fig. 1 Power Input Voltage Configuration

CIRCUIT DESCRIPTION

Channel A input Circuit

The input signal is capacitively coupled via C1 to the divider of R2 and R3. Attenuator switch S6 selects either the full voltage across this divider (X1 position) or only the portion across R3 (approximately one tenth of the full amount, X10 position). This voltage is level-clamped to a maximum of 0.6 volts by transistor Q1,2 and applied to the high-impedance buffer stage. This consists of FET Q3, which provides good sensitivity over the Channel A frequency range, and Q4, which serves as a current source for successive stages.

Channel A Filter

The signal is applied to the low-pass filter consisting of R9 and C9, whose values set a −3 db point of approximately 100 KHz. When LPF switch S7 is pushed in, diodes D1 and D2 are biased on. This provides an ac path to ground through D1, and the filter action of R9 and C9 is enabled. When the switch is released, D1 and D2 are off, isolating C9 from ground, and disabling the filter action.

Channel A Amplifier/Schmitt Trigger

This stage amplifier and shapes the Channel A input to ultimately produce a square wave which is suitable for use in the digital circuits following. The circuit makes use of a 10116 ECL triple line receiver for good response to 100 MHz. Two of the amps in this IC are used to square up the signal, and the third is used as a Schmitt trigger.

The chip supplies a voltage reference of 3.8 volts at pin 11; this is applies through R10,11 and R12,13 to the inputs of the first amp (pins 9 and 16). This results in a quiescent voltage difference of approximately 10 millivolts between the two inputs. This defines the amount of input signal required for proper ''squaring'' to occur in the first two amps.

The third amp, at pins 12 and 13, is used as a Schmitt trigger to eliminate false triggering caused by noise. Its trigger threshold is obtained fromthe pin 11 reference through R20, and the amount of hysteresis is controlled by R21. Transistor Q5 and Q6 are used as ECL-to-TTL level shifters. The waveform obtained across R25 is a 0 to 2.8 volt square wave with polarity opposite that of the Channel A input signal.

Channel B Input Circuit

The input circuit in Channel B consists of amplifiers and divide-by-256 prescaler IC chip. R27 provides a 51 ohm termination for the input jack. The signal from this jack is level-clamped by high-frequency diodes D8 and D9 before application to IC4.

IC4 provide a standard ECL level output and Transistor Q7 and Q8 are used as ECL-to-TTL level shifters. The resulting divided-by-256 signal is fed to the main circuit board via a cable.

Channel A kHz/MHz Select

The TTL level output of channel A is applied to the circuit consisting of NAND gates U13 and U15. U13 input pins 4 and 5 are connected to a line from U4 pins 6 these inputs go low whenever U4 pins 6 engaged. The result is that whenever kHz mode is selected, the kHz signal is gated through to U13 pin 8. At all other times, the MHz (divided by 10). Signal is gated through, when U15 input pins 2 are connected to a line from U2 pins 2, these inputs go high whenever U2 pins 2 engaged.

Divide-by-Ten Circuit

The Channel A output of U13 pin 3 is fed to U14 and U13. U14 is a decade ripple counter which functions as a divide-by-ten. U13 pins 4-13 and U15 pins 1-3 selects either the decade-divided signal from U14 pin 2 or the undivided signal from U13 pin 3. This selection is governed by two lines, one from U4 pins 6, which is high, only during FREQ MHz mode, and one from U2 pin 2, which goes high whenever FREQUENCY MHz mode is selected. This FREQ KHz or MHz selection output (from U13 pin 8) is governed by two lines, one from U1 pin 8, which is high in all modes except TOTALize and one from U2 pin 4, which goes high whenever CHANNEL B mode is selected.

The combined action of U13 and U15, which is controlled by the front panel Function switches, provides U16 with an input signal within its frequency limits. In FREQUENCY MHz mode, the Channel A signal is divided by ten in U14 and applied. In FREQUENCY CHANNEL B mode, the signal from the Channel B jack, scaled down in the IC chip (by 256), and applied. In FREQUENCY kHz, PERiod, and TOTALize modes, the Channel A signal is applied with no frequency division.

CIRCUIT DESCRIPTION

Channel A Signal Gating (TOTALize mode)

One of the inputs to the U15 circuit is a line from U1 pin 8. U1 pin 8 is controlled by two lines, one is U2 pin 10 which goes high in TOTALize mode and the other one is controled by U1 pin 11. The undivided signal from U13 pin 3 is gated additionally by the signals at U1 pins 12 and 13.

U1 pin 12 is controlled by HOLD switch S2 via de-bounce flip-flop U1 pins 1-6. U1 pin 13 is connected via R105 to the rear panel TOTALIZE START/STOP jack. The undivided signal from U13 pin 3 can thus be gated either manually, by S2, or electronically, by a signal applied at the rear panel jack. When no signal is connected to TOTALize jack, the jack is pulled high by R103.

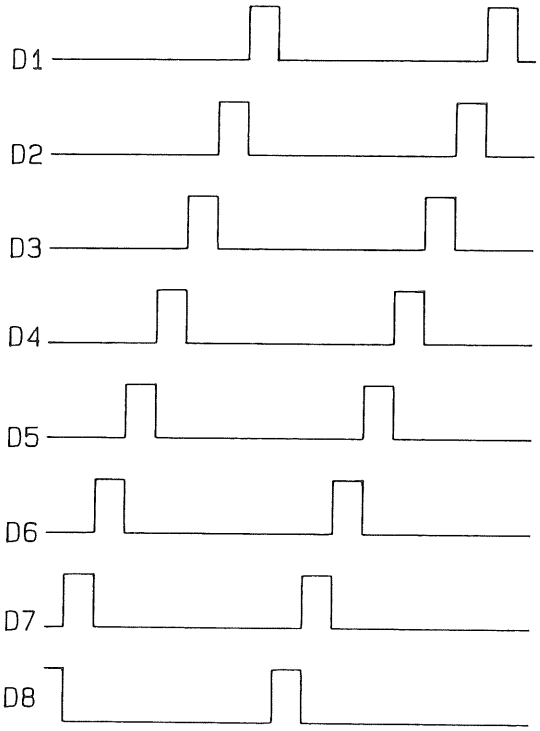
ICM7226A Counter Circuit

This integrated circuit U16 is the heart of the unit. It performs all frequency, period, totalize, check functions and multiplexes drives the displays. It requires an input signal of CMOS digital logic levels, as provided by the circuits previously discussed. A TCXO for the time base is required, as well as external connections for feedback of display digit strobes, as described in the following sections.

Digit Strobes and Feedback

The 7226A multiplexes the display by means of digit strobes D1-D8. Each strobe goes high in sequence, as figure shown in fig. 2, turning its display digit on momentarily. As each digit is selected, the proper seven-segment and decimal point information for that digit is sent out at the same time on pins 8-11 and 13-16.

Fig. 2 digit strobes.

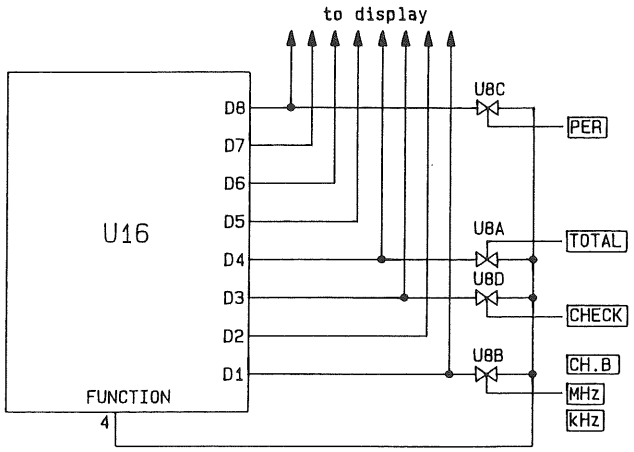


The digit strobes D1-D8 are also used to control the 7226A by selective feedback to four control pins, 1, 4, 20, and 21. Operating mode, resolution, and other parameters are determined by which strobe signal is present at each control input. Strobe feedback is controlled by the control switch of front panel, either directly or through logic. Each control pin and its feedback network is discussed below.

Operating Mode Selection

Operating mode selection is controlled by FUNCTION pin 4. As figure shown in Fig. 3, this pin is connected to one of digit strobes D1, D3, D4 or D8 via bilateral switches U8A to U8D. Which is controlled by FUNCTION switch S3 via U2.

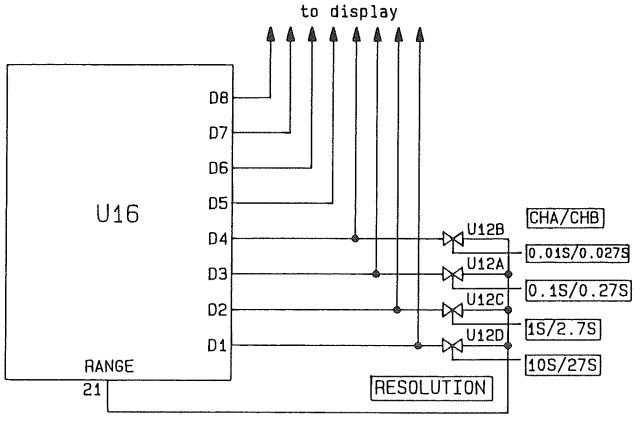
Fig. 3



Resolution Selection

Resolution selection is controlled by RANGE pin 21. As figure shown in fig. 4, digit strobes D1-D4 are applied directly to pin 21 via Bilateral switches U12, Which are controlled by GATE switch S4 via U6.

Fig. 4

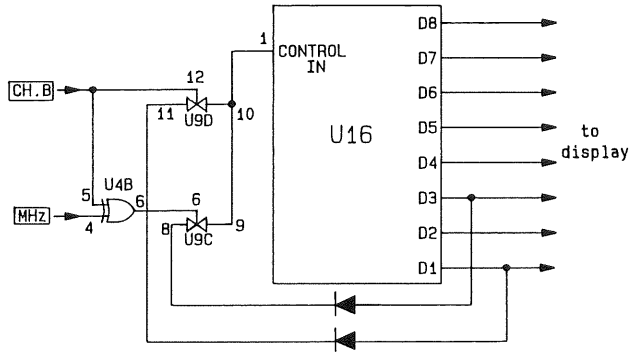


CIRCUIT DESCRIPTION

Additional Control-Pin1

Additional control of U16 is provided by feedback of strobes D1, and D3 to CONTROL IN (PIN 1), as figure shown in fig. 5. This feedback is accomplished through the use of bilateral switches which provides a low-resistance path from input to output (pin 8 to pin 9, or pin 11 to pin 10) when its control input (pin 6 or 12) is high. These two strobesare connected to pin 1 whenever CHANNEL B mode is selected. D3 is gated by U4 pin 6, which goes high whenever either FREQUENCY MHz or CHANNEL B is engaged. The next two sections describe the effects of connecting strobes D1, and D3 to U16 pin 1.

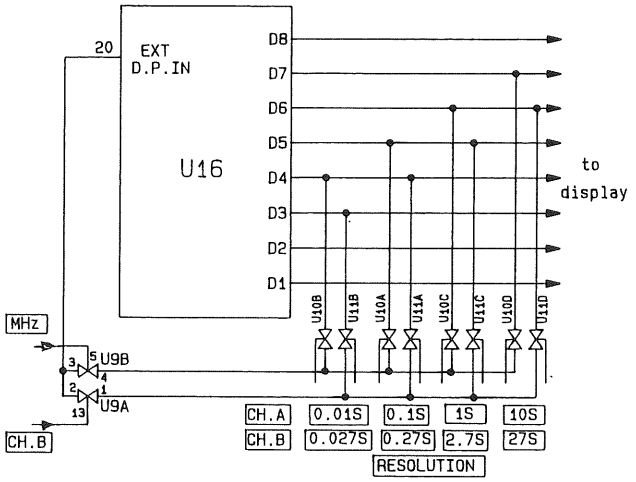
Fig. 5 Additional strobe feedback U16 pin 1



External Decimal Point

Decade division of the input signal occurs at least once in the model, the effect of these divisions is compensated by shifting of the decimal point in the display. This is accomplished by connecting digit strobes D3 to U16 pin 1, as figure shown in fig. 6. In FREQUENCY kHz, PERiod, CHECK and TOTALize modes, D3 is not applied, and automatic decimal point placement is enabled in U16. However, when FREQUENCY MHz or CHANNEL B is engaged, application of D3 instructs U16 to place a decimal point at the display digit whose strobe appears at pin 20, EXT D.P. IN. Placement is determined as figure shown in page 10, and depends on resolution and operating mode selected.

Fig. 6 External decimal point control



Time Base

Channel A and B time base signal are provided by Two separated temperature-compensated crystal oscillator for increased temperature stability. As shown on the schematic diagram, the 10 MHz TCXO is for Channel A and connected to the oscillator input of U16 (pin 35) via U17 pin 1-3 and pin 11-13, which Buffer the TCXO output to a level suitable for driving U16, The other 3.90625 MHz TCXO is for Channel B and connected to the EXT OSC input terminal (pin33) of U16, The 3.90625 MHz TCXO is required to offset the effect of prescaling the input by 256 in the Channel B input circuit.

HOLD Switch

Refer to the schematic diagram. The HOLD switch S2 is connected via U1 pins 1-6, which provides switch debouche, to U16 and U1 pins 8-13. The connection to U16 instructs that chip to enter the display HOLD mode whenever the switch is engaged. In TOTALize operation, however, U16 would freeze only the display but keep on counting, this is remedied by also connecting S2 to U1 pins 8-13. As described previously, this cuts off the input from U16 (as does a low at the TOTALize START/STOP jack), and halts the counting process.

LED Indicators

The MHz indicator, D24, is connected to the output of U4 pin 6. This output, usedinother sections as previously described, goes high when FREQUENCY MHz or CHANNEL B mode is selected.

The kHz/us indicator, D25, is connected via U4 pins 1-3 to the FREQUENCY kHz and PERIOD selected. It lights when either of those modes is selected.

The GATE indicator, D26, is connected via U7 pins 15, to U16 pin 3.
This pin goes low whenever a measurement is in progress. The kHz, MHz, CH.B, PER, TOTAL, CHECK. indicator, (LED1-LED6). is connected via U5 pin 2-7 and pin 9-12, 14-15, U5 buffers the output of U2, The gate time indicators are drived by U7, Which is connected to U6 output.

POWER SUPPLY

The transformer is a universal type whose primary windings may be rewired for various line voltages by rear panel selector switch S8 and S9.

The output of the secondary side is rectified by D110, D111, D113, and D114, and filtered by C120 and C124. Regulator Q9 and Q10 provide + 5 V volts with good regulation and adequate power for the TTL portion of the instrument.

BLOCK DIAGRAM

Refer to the block diagram (as fig. 7) for an overall view of circuit operation. The Frequency counter are designed around an ICM7226A counter chip U16, which performs all frequency, period, totalization counting and check function.

Before being applied to the 7226A, the Channel A input signal is processed by a high-impedance FET input buffer (including a selectable X10 attenuator), a selectable low-pass filter, and an amplifier/Schmitt trigger circuit which squares up the signal.

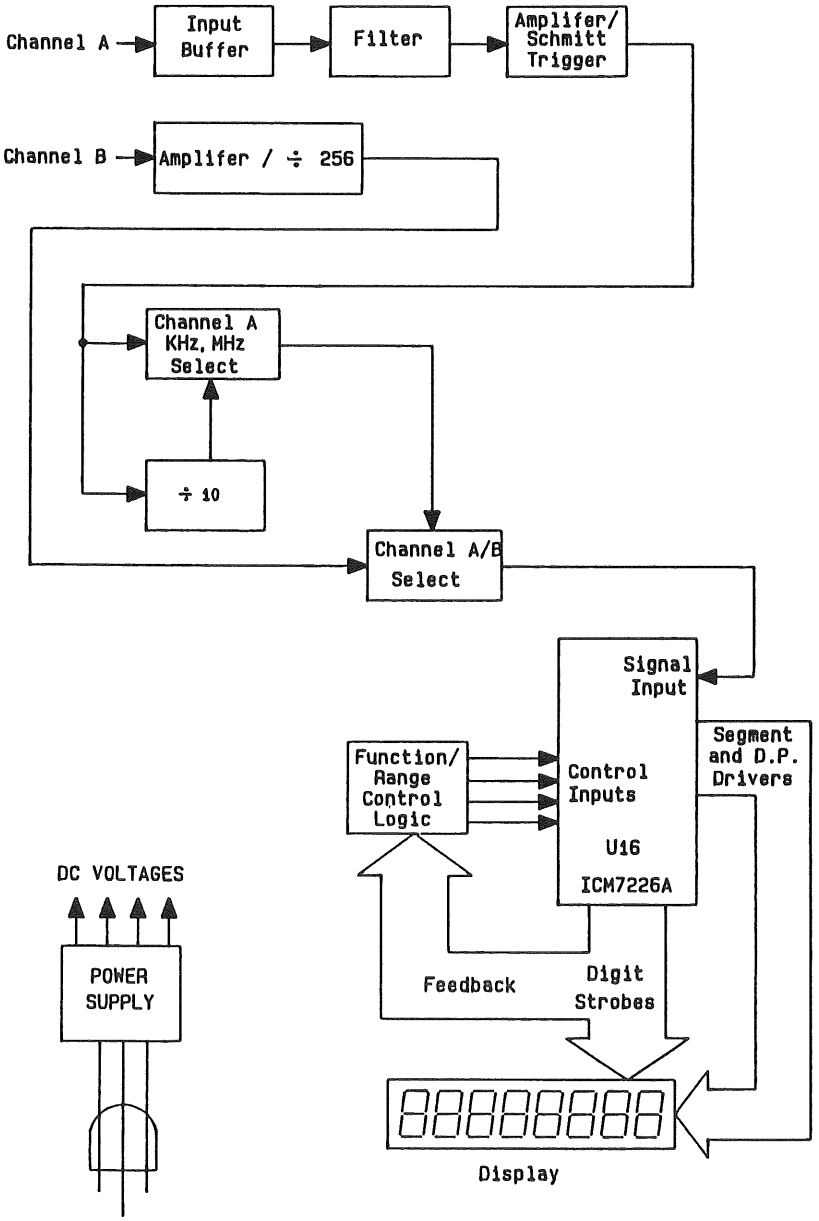
The Channel B input is processed by a high-frequency amplifier and prescaler, which divides the incoming frequency by 256. These divisions in input frequency are offset by a decimal point shift.

According to operating mode, either the Channel A or Channel B signal is selected and applied to the 7226A, either directly or via a divide-by-ten circuit.

Four control inputs on the 7226A determine operating mode, resolution, time base frequency, and decimal point placement. As the diagram shows, selected time-multiplexed digit strobes are fed back to these control inputs via the front panel switches. The controlinputs set operating conditions according to which strobes are applied.

The power supply provides regulated dc voltages. the tapped, dual- primary transformer is universal, and can be rewired as needed to accommodate various line voltages.

Fig. 7 Block Diagram



ADJUSTMENT

1. TCXO Time Base

The model utilize two temperature-compensated crystal oscillator for exceptional temperature stability. Because of the high accuracy of the TCXO, a 10 MHz frequency standard of accuracy at least 1 part in 10000000 is required for calibration. However, if a proper frequency standard is available, calibration is accomplished as follows,

a. With power disconnected, remove the rubber seal from the top case.
b. Reconnect power to the unit,warm up for at least 30 minutes.
c. Connect a 10 MHz frequency standard of accuracy at least 1 part in 10000000 to the Channel A input jack. Select FREQUENCY KHz modeand 1s gate time.
d. Using a non-metallic alignment tool, adjust through the channel A time base adjust hole of the top case and the hole of the TCXO shield for a display of 10,000000.
e. Connect a 1000 MHz frequency standard of accuracy at least 1 part in 10000000 to the Channel B input jack. Select FREQUENCY CH. B mode, and 2.7s gate time.
f. Adjust through the channel B time base adjust hole of the top case and the hole of the TCXO shield for a display of 1000,0000.
g. Disconnect power and replace rubber seal.

2. Channel A Sensitivity

This calibration adjustment requires a RF sine wave generator capable of 10 mV RMS to 50 mV RMS output into 50 ohms at 100 MHz.

a. Disconnect the unit from ac power. Remove the screws and remove the top case.
b. Connect the ac power and select function at FREQ. MHz mode and gate time at 1 sec.
c. Set RF generator output at 100 MHz, 45 mV RMS. Connect the S.G. output to counter channel A input.
d. Locate adjustment trimmer R10, on the main circuit board. Rotate R10 for the correct readings.
e. Reduce the output level of S.G. and slightly adjust R10 until get the best sensitivity and correct readings.
f. Disconnect ac power and replace the top cover.

3. Totalize Sensitivity Adjust

Set Front Panel Controls as follows,

Func..... Total
Gate..... 2.7s/10s
ATT..... Off
LPF ..... Off

a. Connect a TT1 Level 50 KHz signal source to the rear panel Start/stop input BNC terminal.
b. Adjust R118 clockwise to max., the display reading start accumulate the start/stop input signal.
c. Readjust R118 counter-clockwise until the reading stop accumulate.
d. Disconnect the Totalize Start/Stop input signal.
e. Disconnect AC power and replace the top cover.

TROUBLESHOOTING

The following troubleshooting steps provide a logical procedure for fault isolation. While the procedure cannot, of course, guarantee to pinpoint every possible problem, it will in most cases localize the problem to a certain area.

Most of these troubleshooting steps require removal of the top cover as described previously.

General Fault Isolation

1. **Performance test**

   Test each operating mode by applying an appropriate signal to Channel A and Channel B as directed in Table 1. Frequency accuracy of the signal isn't critical, but amplitude should be adequate to produce stable readings (use caution notto exceedthe maximum Channel B input ratings). On Channel A, the filter, and/or attenuator may be used to stabilize the reading.

2. **Fault Isolation**

   Proceed as follows according to the results of the test:

   a. If no display can be obtained at all, follow the procedure for "NO Display".

   b. If display shows abnormalities such as missing decimal points or unlit segments or digits, follow the procedure for "Abnormal Display".

   c. If display appears normal, but value is incorrect or unstable (in Channel B, Channel A, or both), follow the procedure for "Incorrect or Unstable Display Value".

   d. If problem is not adequately described by any of the above, start at "No Display" and proceed through each step until the difficulty is isolated.

TABLE 1 OPERATIONAL TEST

Input Frequency	Operation Mode	RESOLUTION	Normal (Ideal) Display
10 kHz	FREQUENCY kHz	100 Hz 10 Hz 1 Hz .1 Hz	10.0 10.00 10.000 10.0000*
10 kHz	FREQUENCY MHz	1 kHz 100 Hz 10 Hz 1 Hz	.010 .0100 .01000 .010000*
100 MHz	FREQUENCY CH B	10 kHz 1 kHz 100 Hz 10 Hz	100.00 100.000 100.0000 100.00000**
10 kHz	PERiod	.1 us .01 us .001 us .0001 us	100.0 100.00 100.000 100.0000
10 kHz	TOTALize	not applicable.	Display accumulates, with fifth digit from right changing at approximately 1 Hz.
not required input	CHECK	100 Hz 10 Hz 1 Hz .1 Hz	10000.0 10000.00 10000.000 0000.0000* over lit
Less than 100 Hz	PERiod	.0001 us	over lit***

NOTE:
* : Measurement delay of 10 seconds.
** : Measurement delay of 27 seconds.
***: Measurement delay of at least ten seconds.

TROUBLESHOOTING

No Display

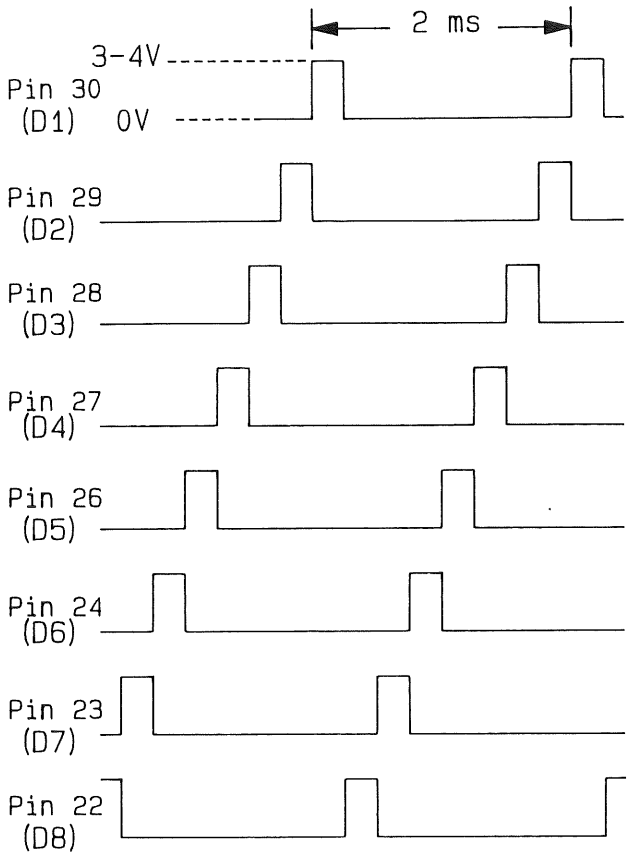
1. Check supply voltage at U16 pin 25 for approximately +5 volts. If this voltage isn't present, check ac input, fuse and +5 V (VA) power supply circuit (D110, D111, C120, Q9). Otherwise proceed to "Abnormal Display".

Abnormal Display

1. **Digit Strobes and time base**

   Set the unit to any operating mode and check for the digit strobe waveforms of fig. 8 at U16 pins 22-24 and 26-30. If these are normal, proceed to step 2. If not, check the output of the time base oscillator at pin 38 for a waveform of frequency 10 MHz and peaks of 0 and 2.4 V. If normal, check U16 and display digits; if no output is obtained, check oscillator components, U16 and +5 V (VB) power supply (D113, D114, C124, Q10).

Fig.8 Digit strobe waveforms from U16



2. **Display test**

   Enable display self-test by connect U16 pins 1 and 22 to each other via a 1N4148 diode (anode to pin 22). Display should be all "eights" with all decimal points and OVERflow indicator on. If not, check displays and U16 segment driver pins 8-11 and 13-16. Waveform ateach of these pins should approximate a dc level of about 1.0 V, with negative spikes of about 4 kHz. Waveforms shown are with display digits connected.

3 **Decimal points**

If the problem involves decimal points in MHz or Channel B modes, check the mode selection logic as in "step 5" of "Incorrect or Unstable Display Value".

4. **MHz or kHz/us indicators**

For problems involving these (D24, D25), check the mode selection logic as in "Incorrect or Unstable Display Value", step 5.

5. **GATE indicator**

If the GATE indicator, D26, does not function properly, check D26, U7 and U16 pin 3. D26 is connected via U7 to pin 3, which goes low whenever a measurement is being taken. (If this pin shows no activity, check for proper mode selection as in "Incorrect or Unstable Display Value", step 5).

6. **Function indicator**

If the Function indicators kHz, MHz, CH B, PER, TOTALize, and CHECK square LEDs, does not function properly, check LED1-LED6, U5 and U2.

7. **Gate time indicator**

If the Gate time indicator. 01/.027s, .1/.27s, 1/2.7s, and 10/27s square LEDs does not function properly, check LED7-LED10, U6 and U7.

Incorrect or Unstable Display Value

1. **Half-splitting: Channel A**

Apply an appropriate signal to Channel A , and check the waveform at the collector of Q6. Waveform should bea square wave (0-2.8 V) of same frequency and polarity as the Channel A input signal. If the waveform is normal, proceed step 3; otherwise, check for a problem in the Channel A analog circuitry; see the next step.

2. **Channel A analog circuits**

Table 2 gives waveforms for the Channel A input buffer and signal shaping circuits, along with input conditions required for obtaining them.The order of table entries is from input to output, permitting either sequential or half-splitting trouble-shooting techniques, as desired by the user.

3. **Half-splitting: Channel B**

Apply an appropriate signal to the Channel jack. Check the output of the ECL-to-TTL converter, collector of Q8.

A TTL level waveform should be observed; its frequency should be 1/256 of input frequency. Note that because of the high frequency, shape irregularities in this waveform can be expected.

If the waveform is correct, proceed to step 5. If not, check the Channel B circuits.

4. **Channel B input amplifier**

With signal still applied at the Channel B input, check for presence of signal at the input of IC4, and the outputof Q7 and Q8. If not detected, check IC4 and associated components.

TABLE 2 CHANNEL A ANALOG CIRCUIT WAVEFORM

Test Point	Waveform (See Note 1 next page)
A. Gate of Q3	Identical to input.
B. Gate of Q3, but with ATTEN set to X10.	1/10 amplitude of input.
C. Source of Q3. Connection point of C8, C9, C11, R9.	1 Vp-p, 10 kHz sine wave centered at +1.3 V.(see Note 2 next page)
D. IC1 pin 10.	1 Vp-p, 10 kHz sine wave centered at +3.8 V.
E. IC1 pin 9, 11	DC level of +3.8 V.
F. IC1 pin 4 or 7.	1 Vp-p, 10 kHz rounded square wave centered at +3.8 V.
G. IC1 pin 5 or 6.	Same as F, but inverted.
H. IC1 pin 3 or 12.	Same as F, with squarer edges.
I. IC1 pin 2.	Same as H, but inverted.
J. IC1 pin 13.	0.7 Vp-p, 10 kHz square wave centered at +3.8 V.
K. IC1 pin 15, or base of Q5.	1 Vp-p, 10 kHz square wave centered at +3.8 V.
L. IC1 pin 14, or base of Q6.	Same as K, but inverted

Note 1. Counter input of 10 kHz, 1 Vp-p sine wave for all measurements except point C; see Note 2 below. All measurements made with ATTenuator set to X1, except point B. LPF may be engaged to eliminate input noise, except point C; see NOTE 2 below.

Note 2. Counter input for point C test is 100 kHz, 1 Vp-p. With LPF switch off, point C waveform should be approximately 1 Vp-p; with LPF on, it should diminish to about 0.7 Vp-p.

5. **Mode selection logic**

Operating mode, resolution, and other factors are determined by feedback of the U16 digit strobes D1-D8 to various control pins of this same chip. This feedback is controlled, either directly or through logic, by the front panel switches. Tables 3 and 4 give normal logic conditions in these feedback connections.

6. **ChannelA kHz/MHz select**

The gates of U13, U15 select either the kHz or MHz signal, according to the logic state of a line from U2 pin 2 to U15 pin 2 and a line from U4 pin 6 to U13 pin 4 and 5. as follow:

a. When the line from U2 pin 2 is high, U13 pin 8 should have a TTL waveform of same frequency as the MHz output.

b. When the line from U4 pin 6 to U13 pin 4 and 5 is low, the TTL frequency at U13 pin 8 should be same as the kHz input. If the waveform is abnormal, check U13 pin 1-6, pin 11-13, U15 pin 1-3.

c. Divide-by-ten. U14 and U13 (and part of U15) form acircuit which divided the signal at U13 pin 3 by 10 and selects either the divided signal or the direct signal for application to U6.

d. The U14 output frequency at pin 2 should be 1/10 that of the input at pin 8 (U13 pin 3). If not check U14.

TABLE 3 CHECK OF DIFFERENT GATE TIME

Front Panel Gate Engaged	Test Points	
Gate Time .01s	U16 pin 21	U16 strobe D1 (pin 30).
	U9 pin 4	U16 strobe D4 (pin 27).
	U9 pin 1	U16 strobe D3 (pin 28).
Gate Time .1s	U16 pin 21	U16 strobe D2 (pin 29).
	U9 pin 4	U16 strobe D5 (pin 26).
	U9 pin 1	U16 strobe D4 (pin 27).
Gate Time 1.0s	U16 pin 21	U16 strobe D3 (pin 28).
	U9 pin 4	U16 strobe D6 (pin 24).
	U9 pin 1	U16 strobe D5 (pin 26).
Gate Time 10s	U16 pin 21	U16 strobe D4 (pin 27).
	U9 pin 4	U16 strobe D7 (pin 23).
	U9 pin 1	U16 strobe D6 (pin 24).

7. **Channel A / Channel B Select**

a. The selection in U15 is controlled by a line from U2 pin 4 (see Table 4), which goes high whenever CH B mode is engaged. When it is high, the output of U15 pin 8 should be selected CH B mode.

b. When the line from U2 pin 4 is low (meaning some mode other than Channel A or B is selected), the frequency at U15 pin 8 should be the same as that at U13 pin 8, except in TOTAL mode, as described in step c.

c. Gating of the direct signal from U13 pin 8 is also controlledby the input to U15 pin 12, which goes high in all modes except TOTALize. In that mode, U15 pin 12 is connected to the output of U1 pins 8. This output should be high when the HOLD switch S2 is disengaged, and no input is applied to rear panel jack. A TTL low is applied to this jack, or if S2 is engaged, U1 pin 8 should go low, disabling U15 pins 11-13 (constant low output). In that event, the output at U15 pin 8 should be a constant low. If these conditions are not normal, check U15, U1, U2 and S2.

8. Reset

Check that all readings are cleared to zero when RESET switch is pushed. If not, check S1.

TABEL 4 Check of Function Logic

Function Engaged	Test Points	Waveform
Frequency kHz	U16 pin 4 U4 pin 1, 3 D25 U2 pin 3	U16 strobe D1 (pin 30). Logic high. Lit. Logic high.
Frequency MHz	U16 pin 4 U9 pin 5 U9 pin 3 U16 pin 20 U4 pin 4 U2 pin 2	U16 strobe D1 (pin30). Logic high. Same as U9 pin 4 (U16 digit strobe selected by Gate switch, see Table 3). Logic high. Logic high (see other entries for U4 pin 6).
Frequency CH B	U16 pin 4 U9 pin 12,13 U9 pin 2 U16 pin 20 U9 pin 9,10 U4 pin 5 U4 pin 6 U15 pin 4 U2 pin 4	U16 strobe D1 (pin 30). Logic high. Same as U9 pin 1 (U16 digit strobe selected by Gate switch, see Table 3). See last entry in this table. Logic high. Logic high (see other entries for U4 pin 6). Logic high (see step 6 of "Incorrect or Unstable Display Value" procedure). Logic high.
PERiod	U16 pin 4 U4 pin 11,12 D25 U2 pin 7	U16 strobe D8 (pin 22). Logic high. Lit. Logic high.
TOTALize	U16 pin 4 U1 pin 9 U2 pin 10	U16 strobe D4 (pin 27). Same as U1 pin 8 and U15 pin 12 Logic high.
CHECK	U16 pin 4 U4 pin 13 U2 pin 1	U16 strobe D3 (pin 28). Logic high. Logic high.
Either Frequency MHz or Frequency CH B	U4 pin 6 D24 U9 pin 6	Logic high. Lit. Logic high.

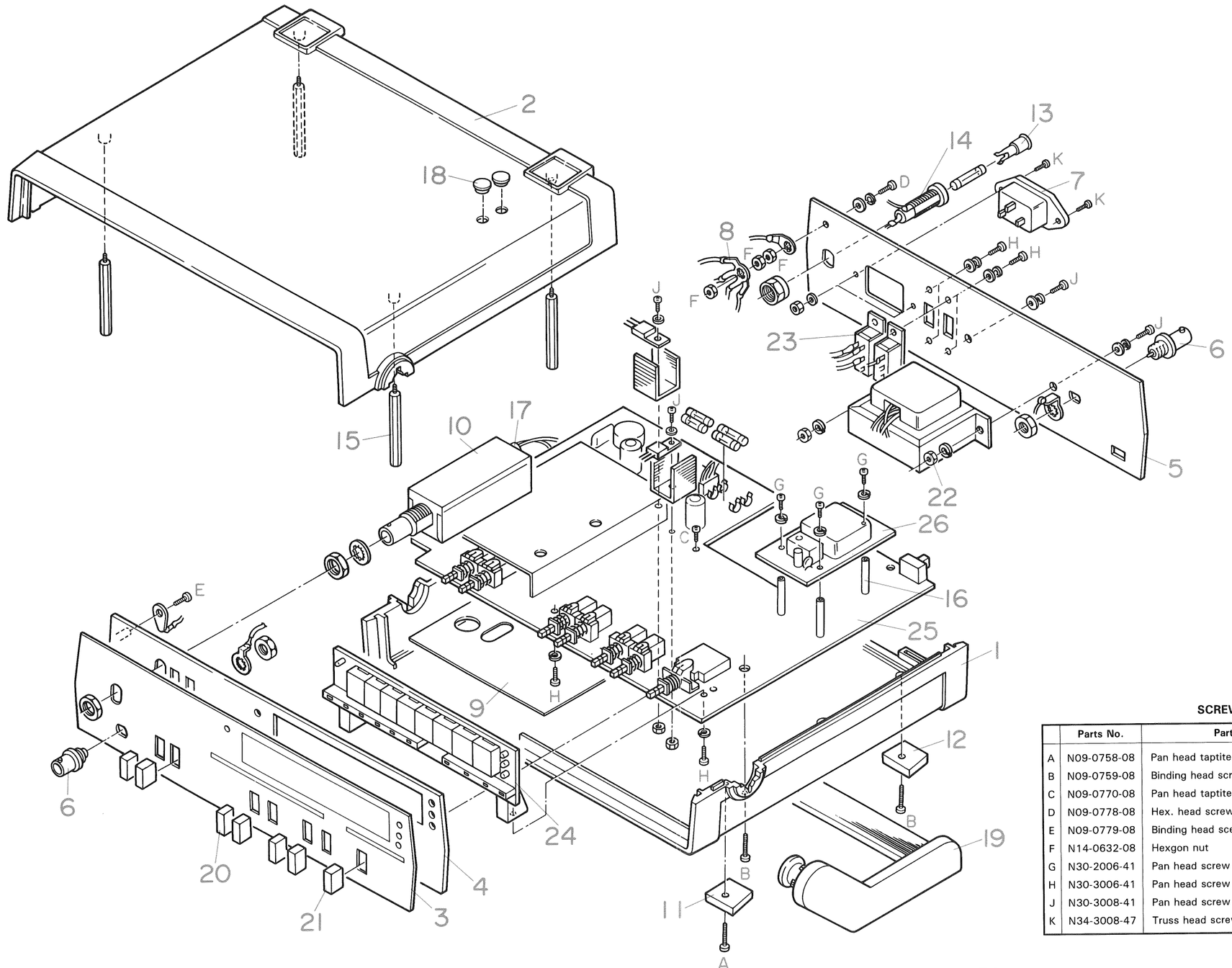
PARTS LIST

FC-758 UNIT

(Y81-1060-00)

REF.NO	PARTS NO	NAME & DESCRIPTION
	B41-0870-08	FUSE CAUTION LABEL
	B42-3693-08	SERIAL LABEL
	B50-7727-00	INSTRUCTION MANUAL,JAPANESE
	B50-7728-00	INSTRUCTION MANUAL,ENGLISH
	E30-1644-15	BS POWER CORD
	E30-1818-05	JIS POWER CORD SET
	E30-1819-05	CEE POWER CORD
	E30-1820-05	UL/CSA POWER CORD
	F51-0001-05	FUSE(SLOW BLOW) 250V 0.25A
	F51-0002-05	FUSE(SLOW BLOW) 250V 0.125A
	G02-0612-08	COIL SPRING
	G13-0733-08	SPONGE
	H01-5913-08	CARTON BOX
	H12-0571-08	FOAMED PAD
	H20-1728-08	VIYNL COVER 320X340X0.06
1	A02-0523-08	BOTTOM CASE
2	A02-0531-08	TOP CASE
3	A21-1167-08	OVERLAY
4	A22-0879-08	FRONT PANEL
5	A23-1702-08	BACK PANEL
6	E04-0264-08	BNC CONNECTOR
7	E18-0351-05	AC INLET 3 P
8	E22-0282-08	4 LEG LUG
9	F10-1629-08	SHIELD PAPER
10	F10-1632-08	SHIELD COVER
11	J02-0520-08	RUBBER FOOT(FRONT)
12	J02-0521-08	RUBBER FOOT(REAR)
13	J13-0515-08	FUSE CARRIER
14	J13-0516-08	FUSE BASE
15	J32-0882-08	HEX. STUD L=44.2
16	J32-0896-08	HEX. STUD
17	J42-0553-08	SNAP BUSHING
18	J42-0555-08	RUBBER PLUG
19	K01-0527-08	HANDLE
20	K27-0542-08	PUSH KNOB,WHITE WHITE
21	K27-0557-08	PUSH KNOB,ORANGE
22	L01-9949-08	POWER TRANSFORMER
23	S31-1510-08	SLIDE SWITCH
24	W02-0490-08	DISPLAY UNIT
25	W02-0493-08	MAIN UNIT
26	W02-0495-08	TCXO UNIT
27	W02-0496-08	CH 8 UNIT

DISASSEMBLY



SCREWS

	Parts No.	Parts Name		Figure
A	N09-0758-08	Pan head taptite screw	(3.5×8)	
B	N09-0759-08	Binding head screw	(6/32inch×18)	
C	N09-0770-08	Pan head taptite screw	(3.5×6)	
D	N09-0778-08	Hex. head screw	(M3.5×6)	
E	N09-0779-08	Binding head scew	(M3.5×6)	
F	N14-0632-08	Hexgon nut	(M3.5)	
G	N30-2006-41	Pan head screw	(M2×6)	
H	N30-3006-41	Pan head screw	(M3×6)	
J	N30-3008-41	Pan head screw	(M3×8)	
K	N34-3008-47	Truss head screw	(M3×8)	

FC-758

PARTS LIST

DISPLAY UNIT
(W02-0490-08)

REF.NO	PARTS NO	NAME & DESCRIPTION
	J19-1667-08	LED HOLDER
	J19-1668-08	LED HOLDER
	J73-0002-08	PCB (UNMOUNTED)
D024	B30-0976-08	LED LAMP;ORANGE
D025	B30-0976-08	LED LAMP;ORANGE
D026	B30-0976-08	LED LAMP;ORANGE
D027	B30-0976-08	LED LAMP;ORANGE
DS001	B30-0975-08	LED DISPLAY
DS002	B30-0975-08	LED DISPLAY
DS003	B30-0975-08	LED DISPLAY
DS004	B30-0975-08	LED DISPLAY
DS005	B30-0975-08	LED DISPLAY
DS006	B30-0975-08	LED DISPLAY
DS007	B30-0975-08	LED DISPLAY
DS008	B30-0975-08	LED DISPLAY
LED001	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED002	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED003	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED004	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED005	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED006	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED007	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED008	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED009	B30-0977-08	LED LAMP;SQUARE.ORANGE
LED010	B30-0977-08	LED LAMP;SQUARE.ORANGE

MAIN UNIT
(W02-0493-08)

REF.NO	PARTS NO	NAME & DESCRIPTION			
	E02-0155-08	IC SOCKET	14 PIN		
	E18-0351-05	AC INLET	3 P		
	E23-0584-08	PIN			
	E38-0001-08	WIRE ASS'Y:DISPLAY TO MAIN GND			
	E38-0003-08	WIRE ASS'Y:JA.JB.JD TO DISPLAY			
	E38-0004-08	WIRE ASS'Y:JC TO DISPLAY PCB			
	E38-0006-08	WIRE ASS'Y:G1S1 TO CH B BNC			
	F01-0880-08	HEAT SINK			
	F10-1630-08	SHIELD CASE			
	J13-0514-08	FUSE CLIP			
	J73-0003-08	PCB (UNMOUNTED)			
	L01-9949-08	POWER TRANSFORMER			
C001	CF93AN2E473K	CAP. POLYESTER	0.047	10%	250V
C002	CC45CH2H010C	CAP. CERAMIC	1P	0.25P	500V
C003	CC45CH2H120J	CAP. CERAMIC	12P	5%	500V
C004	CM93BF2H131J	CAP. MICA	130P	5%	500V
C005	CK45B1H103K	CAP. CERAMIC	0.01	10%	50V
C006	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C007	NO USE				
C008	CM93BF2H131J	CAP. MICA	130P	5%	500V
C009	CK45B1H103K	CAP. CERAMIC	0.01	10%	50V
C010	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C011	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C012	CK45B1H103K	CAP. CERAMIC	0.01	10%	50V
C013	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C014	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C015	CC45SL1H471J	CAP. CERAMIC	470P	5%	50V
C101	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C102	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C103	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C104	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C105	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C106	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C107	CC45CH2H390J	CAP. CERAMIC	39P	5%	500V
C114	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C115	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C116	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C117	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C118	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C119	CK45B1H103K	CAP. CERAMIC	0.01	10%	50V
C120	CE04EW1V102M	CAP. ELECTRO	1000	20%	35V
C121	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C122	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C123	CK45B1H103K	CAP. CERAMIC	0.01	10%	50V
C124	CE04EW1V102M	CAP. ELECTRO	1000	20%	35V
C125	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C126	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
C127	C91-1321-08	CAP. POLYESTER	0.22	10%	630V
C128	C91-1320-08	CAP. CERAMIC	0.001	20%	4KV
C129	C91-1320-08	CAP. CERAMIC	0.001	20%	4KV
C130	CK45F1H104Z	CAP. CERAMIC	0.1		50V
D001	1N4148	DIODE			
D002	1N4148	DIODE			
D101	1N4007	DIODE			
D102	1N4007	DIODE			
D103	1N4148	DIODE			
D104	1N4148	DIODE			
D105	1N4148	DIODE			
D106	1N4148	DIODE			
D107	1N4148	DIODE			
D108	1N4148	DIODE			
D109	1N4148	DIODE			
D110	1N4004	DIODE			
D111	1N4004	DIODE			
D112	1N4148	DIODE			
D113	1N4004	DIODE			
D114	1N4004	DIODE			
D115	1N4148	DIODE			
FS001	F50-0001-08	FUSE(5X20MM) 0.5A 250V			
FS002	F50-0001-08	FUSE(5X20MM) 0.5A 250V			
FS003	F50-0001-08	FUSE(5X20MM) 0.5A 250V			
FS004	F50-0001-08	FUSE(5X20MM) 0.5A 250V			
IC001	MC10116P	IC, TRIPLE LINE RECEIVER			
JA	E40-7103-08	PIN CONNECTOR	8P		
JB	E40-7103-08	PIN CONNECTOR	8P		
JC	E40-7104-08	PIN CONNECTOR	9P		
JD	E40-7103-08	PIN CONNECTOR	8P		
JE	E40-7029-08	PIN CONNECTOR	3P		

PARTS LIST

REF.NO	PARTS NO	NAME & DESCRIPTION			
JF	E40-7074-08	PIN CONNECTOR	6P		
J101	R92-0150-05	JUMPING RES.	ZERO OHM(10MM)		
L001	L39-0532-08	COIL			
Q001	2SC1674(K)	TR. SI, NPN			
Q002	2SC1674(K)	TR. SI, NPN			
Q003	2N5486	FET, N-CHANNEL			
Q004	MPS3640	TR. SI, PNP			
Q005	MPS3640	TR. SI, PNP			
Q006	MPS3640	TR. SI, PNP			
Q009	HA17805P	IC, FIXED VOLTAGE REGULATOR			
Q010	HA17805P	IC, FIXED VOLTAGE REGULATOR			
Q011	2SC1815(GR)	TR. SI, NPN			
R001	RD14BB2E5R1J	RES. CARBON	5.1	5%	1/4W
R002	RN14BK2E1104F	RES. METAL FILM	1.1M	1%	1/4W
R003	RN14BK2E1213F	RES. METAL FILM	121K	1%	1/4W
R004	RD14DB2H101J	RES. CARBON	100	5%	1/2W
R005	RD14BB2E104J	RES. CARBON	100K	5%	1/4W
R006	RN14BK2E1300F	RES. METAL FILM	130	1%	1/4W
R007	RD14BB2E100J	RES. CARBON	10	5%	1/4W
R008	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R009	RD14BB2E151J	RES. CARBON	150	5%	1/4W
R010	R12-3041-05	RES. SEMI FIXED	10KB		
R011	RD14BB2E104J	RES. CARBON	100K	5%	1/4W
R012	RD14BB2E222J	RES. CARBON	2.2K	5%	1/4W
R013	RD14BB2E222J	RES. CARBON	2.2K	5%	1/4W
R014	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R015	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R016	RD14BB2E181J	RES. CARBON	180	5%	1/4W
R017	RD14BB2E331J	RES. CARBON	330	5%	1/4W
R018	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R019	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R020	RD14BB2E331J	RES. CARBON	330	5%	1/4W
R021	RD14BB2E151J	RES. CARBON	150	5%	1/4W
R022	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R023	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R024	RD14BB2E220J	RES. CARBON	22	5%	1/4W
R025	RD14BB2E750J	RES. CARBON	75	5%	1/4W
R026	RN14BK2E4120F	RES. METAL FILM	412	1%	1/4W
R045	RD14BB2E221J	RES. CARBON	220	5%	1/4W
R101	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R102	RD14BB2E302J	RES. CARBON	3K	5%	1/4W
R103	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R104	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R105	RD14BB2E101J	RES. CARBON	100	5%	1/4W
R106	RD14BB2E474J	RES. CARBON	470K	5%	1/4W
R107	RD14BB2E474J	RES. CARBON	470K	5%	1/4W
R108	RD14BB2E104J	RES. CARBON	100K	5%	1/4W
R109	RD14BB2E181J	RES. CARBON	180	5%	1/4W
R110	RD14BB2E471J	RES. CARBON	470	5%	1/4W
R111	RD14BB2E361J	RES. CARBON	360	5%	1/4W
R112	RD14BB2E361J	RES. CARBON	360	5%	1/4W
R113	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R114	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R115	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R116	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R117	RD14BB2E181J	RES. CARBON	180	5%	1/4W
R118	R12-7512-08	RES. SEMI FIXED	500KB		
R119	NO USE				
R120	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R121	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R122	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R123	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
R127	RD14BB2E103J	RES. CARBON	10K	5%	1/4W
S001	S40-1533-08	PUSH SWITCH			
S002	S42-2518-08	PUSH SWITCH			
S003	S40-1533-08	PUSH SWITCH			
S004	S40-1533-08	PUSH SWITCH			
S005	S40-2524-05	PUSH SWITCH (POWER)			
S006	S40-2519-08	PUSH SWITCH			
S007	S40-2519-08	PUSH SWITCH			
TP001	E23-0583-08	TEST PIN			
U001	HD74LS00P	IC, QUAD 2 INPUT NAND			
U002	HD14017BP	IC, DECADE COUNTER/DIVIDER			
U003	HD74LS00P	IC, QUAD 2 INPUT NAND			
U004	HD74LS86P	IC, QUAD 2 INPUT EX-OR			
U005	MC14049UBCP	IC, HEX INVERTER/BUFFER			
U006	HD14017BP	IC, DECADE COUNTER/DIVIDER			
U007	MC14049UBCP	IC, HEX INVERTER/BUFFER			
U008	HD14066BP	IC, QUAD ANALOG SW/QUAD MPX			
U009	HD14066BP	IC, QUAD ANALOG SW/QUAD MPX			
U010	HD14066BP	IC, QUAD ANALOG SW/QUAD MPX			
U011	HD14066BP	IC, QUAD ANALOG SW/QUAD MPX			
U012	HD14066BP	IC, QUAD ANALOG SW/QUAD MPX			
U013	SN74S00N	IC, QUAD. 2-NAND			
U014	SN74S196	IC, PRESETTABLE DECADE COUNTER			
U015	CD74HCT00	IC, QUAD 2 INPUT NAND			
U016	ICM7226AIJL	IC,8-DIGIT FREQ. COUNTER/TIMER			
U017	MC74HC00	IC, QUAD 2 INPUT NAND			

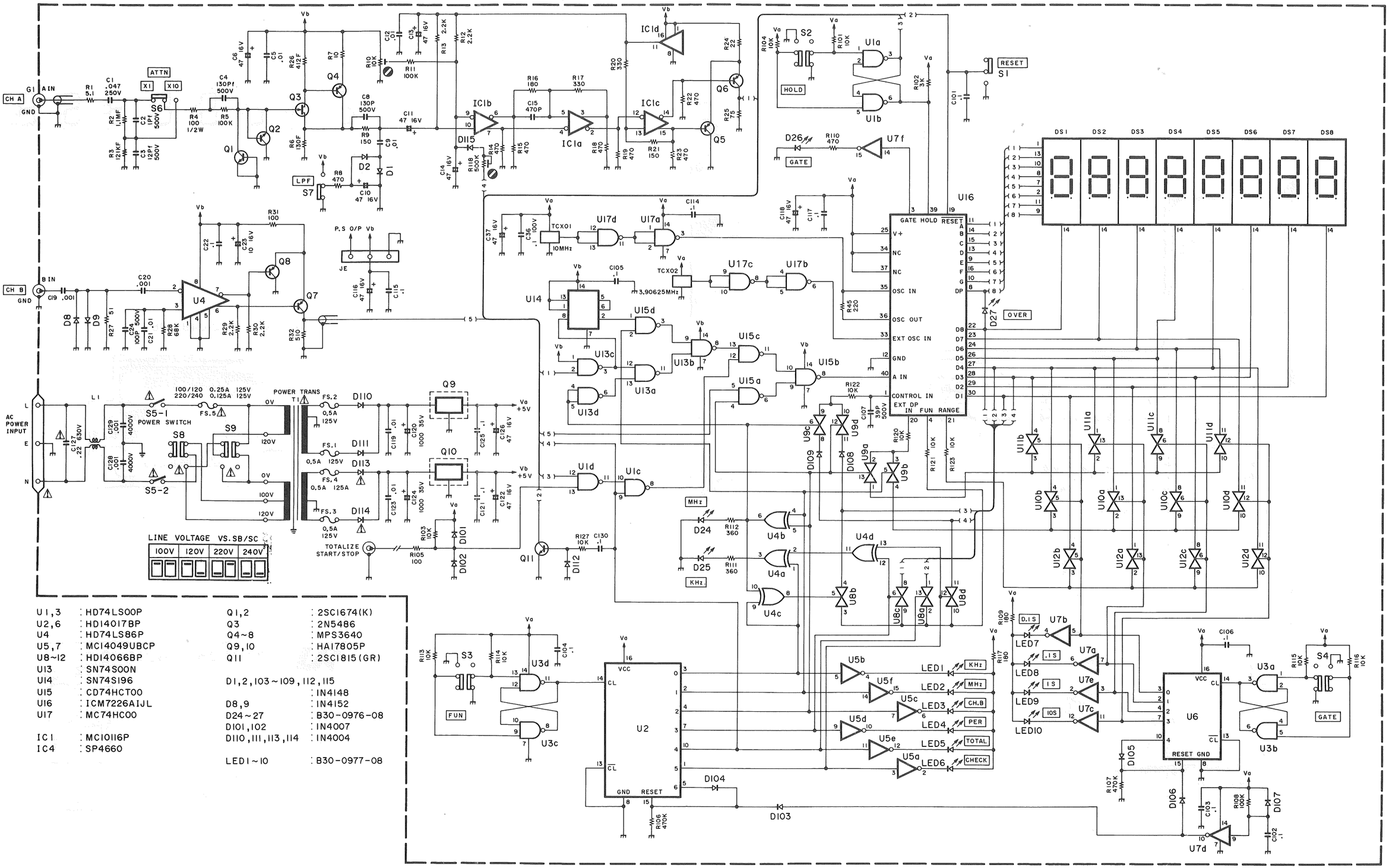
TCXO UNIT
(W02-0495-08)

REF.NO	PARTS NO	NAME & DESCRIPTION			
	E38-0002-08	WIRE ASS'Y:MAIN TO TCXO J117			
	J73-0005-08	PCB (UNMOUNTED)			
	L77-1040-05	CRYSTAL RESONATOR (10MHZ)			
	L77-1041-05	CRYSTAL RESONATOR (3.90625MHZ)			
C036	CK45B2A103K	CAP. CERAMIC	0.01	10%	100V
C037	CE04EW1C470M	CAP. ELECTRO	47	20%	16V
J117	E40-7105-08	PIN CONNECTOR	5P		

CHANNEL B UNIT
(W02-0496-08)

REF.NO	PARTS NO	NAME & DESCRIPTION			
	E04-0264-08	BNC CONNECTOR			
	E38-0005-08	WIRE ASS'Y:CH B PCB TO JE			
	F10-1631-08	SHIELD CASE			
	J73-0001-08	PCB (UNMOUNTED)			
C019	CK45B1H102K	CAP. CERAMIC	1000P	10%	50V
C020	CK45B1H102K	CAP. CERAMIC	1000P	10%	50V
C021	CK45F1H103Z	CAP. CERAMIC	0.01		50V
C022	CK45F1H104Z	CAP. CERAMIC	0.1		50V
C023	CE04CW1C100M	CAP. ELECTRO	10	20%	16V
C024	CK45B2H101K	CAP. CERAMIC	100P	10%	500V
D008	1N4152	DIODE			
D009	1N4152	DIODE			
IC004	SP4660	IC,PRESCALER			
Q007	MPS3640	TR. SI, PNP			
Q008	MPS3640	TR. SI, PNP			
R027	RD14BB2E510J	RES. CARBON	51	5%	1/4W
R028	RD14BB2E683J	RES. CARBON	68K	5%	1/4W
R029	RD14BB2E222J	RES. CARBON	2.2K	5%	1/4W
R030	RD14BB2E222J	RES. CARBON	2.2K	5%	1/4W
R031	RD14BB2E101J	RES. CARBON	100	5%	1/4W
R032	RD14BB2E511J	RES. CARBON	510	5%	1/4W

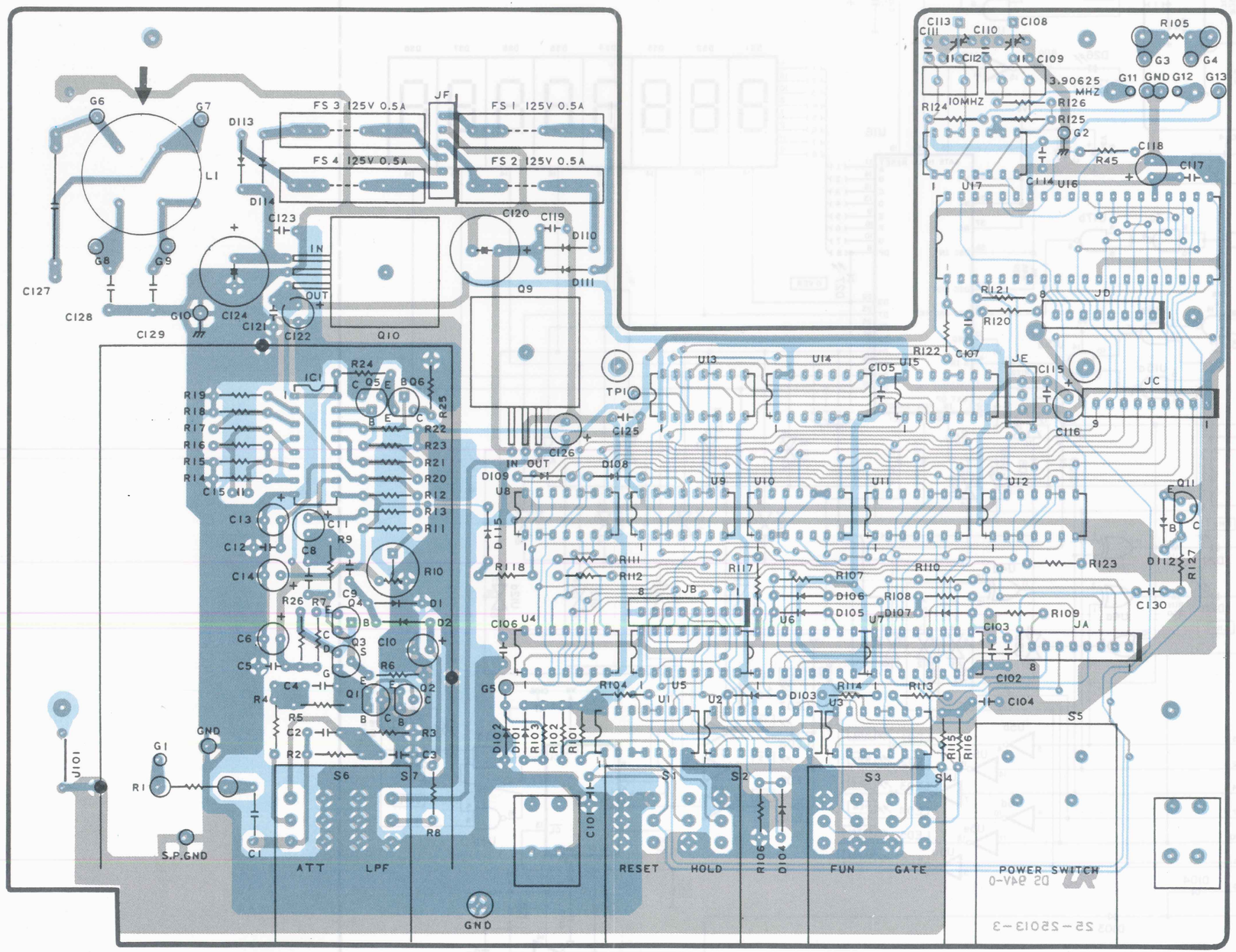
SCHEMATIC DIAGRAM



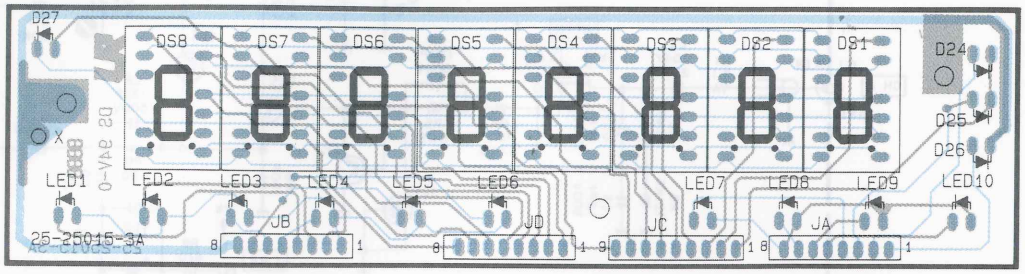
U1,3	: HD74LS00P	Q1,2	: 2SC1674(K)
U2,6	: HDI4017BP	Q3	: 2N5486
U4	: HD74LS86P	Q4~8	: MPS3640
U5,7	: MCI4049UBCP	Q9,10	: HAI7805P
U8~12	: HDI4066BP	Q11	: 2SC1815(GR)
U13	: SN74S00N		
U14	: SN74S196	D1,2,103~109,112,115	: IN4148
U15	: CD74HCT00		
U16	: ICM7226AIJL	D8,9	: IN4152
U17	: MC74HC00	D24~27	: B30-0976-08
		D101,102	: IN4007
IC1	: MCI0116P	D110,111,113,114	: IN4004
IC4	: SP4660		
		LED1~10	: B30-0977-08

FC-758

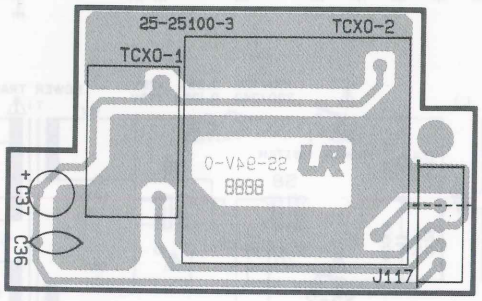
MAIN UNIT (W02-0493-08)



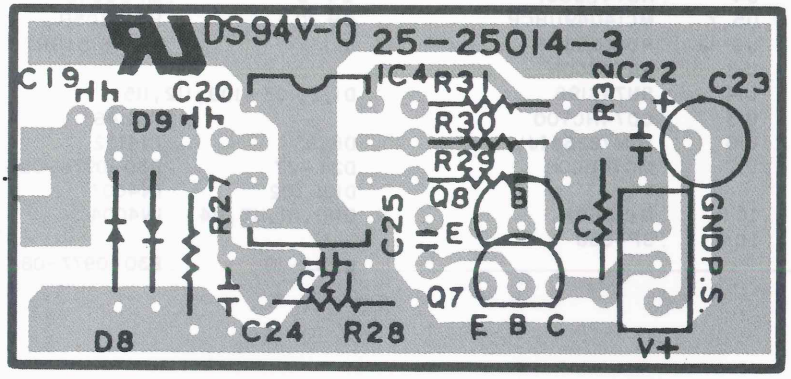
DISPLAY UNIT (W02-0490-08)



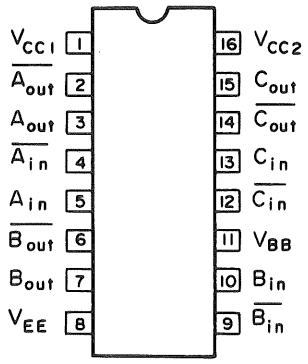
TCXO UNIT (W02-0495-08)



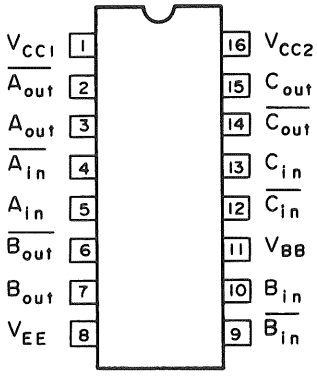
CHANNEL B UNIT (W02-0496-08)



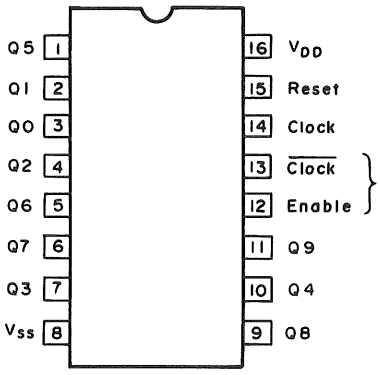
SEMICONDUCTORS



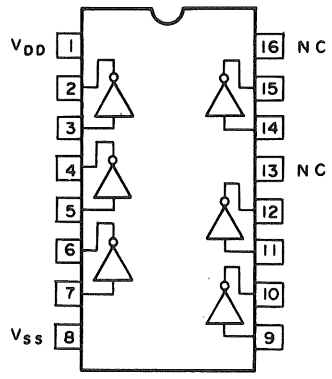
MC10116P



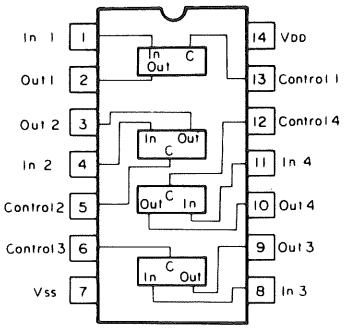
MC10216P



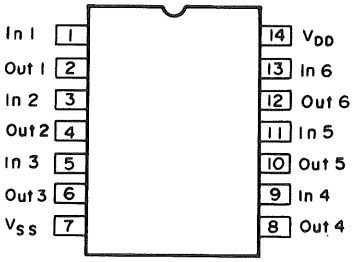
MC14017BCP
HD14017BD



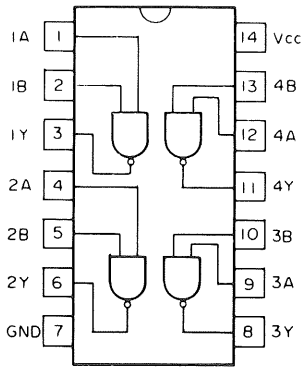
MC14049uBCP



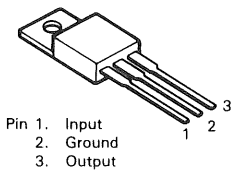
MC14066BCP
HD14066BP



MC14069BCP

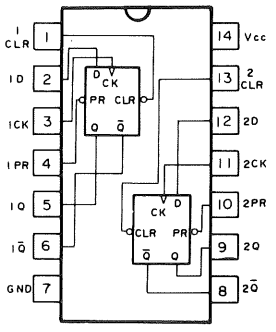


MC74HC00
SN74S00N
SN74LS00N
CD74HCT00
HD74LS00P



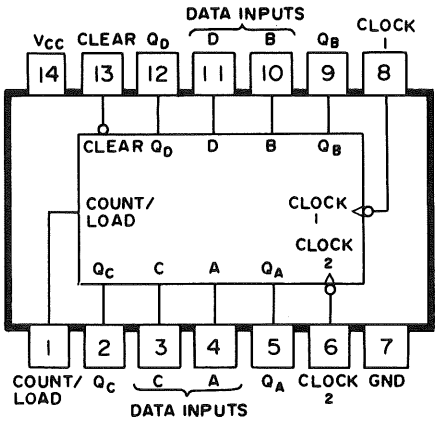
Pin 1. Input
2. Ground
3. Output

MC7805CT

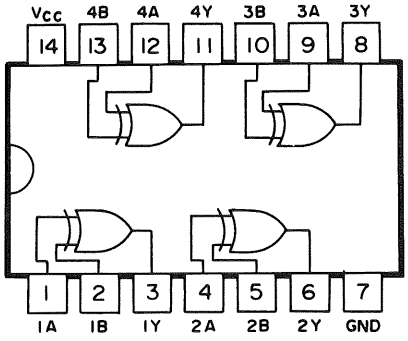


SN74ALS74AN

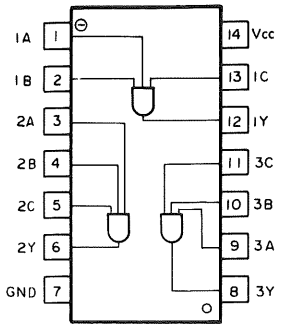
SEMICONDUCTORS



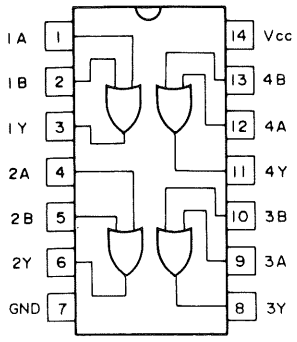
SN74S196



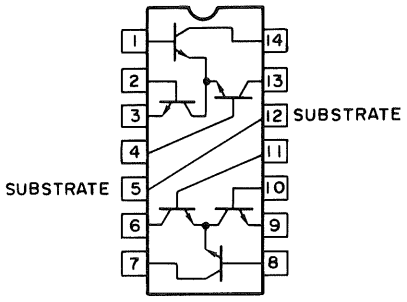
CD74HCT86E
HD74LS86P



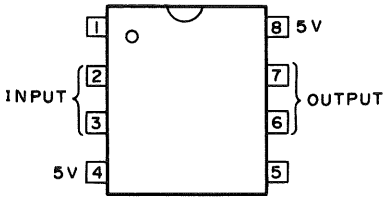
HD74LS11P



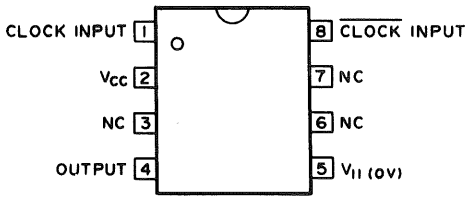
HD74LS32P



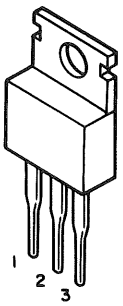
CA3102E



SP4660

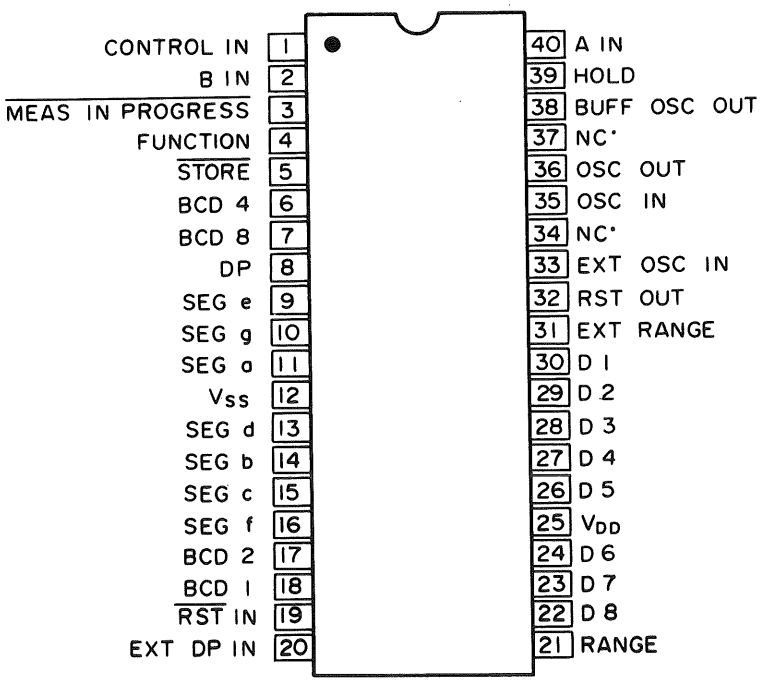


SP8660



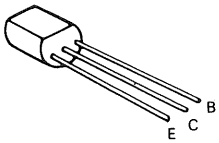
1. Input
2. Ground
3. Output

HA17805P

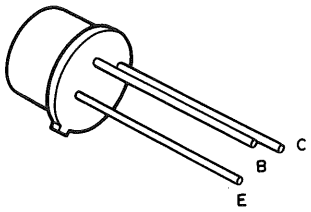


ICM7226AIJL

SEMICONDUCTORS



2SC535C
2SC1674(K)
2SC1815(GR)



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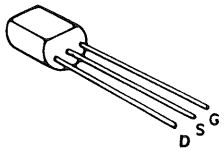
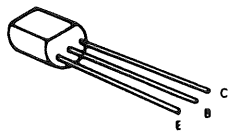


2N5486



MPS3640

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